In the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1.-24. (Canceled)

25. (New) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion for reading in a computational instruction;

a decoding portion for decoding the computational instruction that has been read in;

an execution portion for executing the computational instruction in accordance with a decoding of the computational instruction; and

an instruction overriding control circuit for controlling an overriding of subsequent instructions that follow the computational instruction in response to a conditional execution status updated by a sequencer in accordance with the decoding of the computational instruction.

26. (New) The data processing device according to claim 25, wherein the instruction overriding control circuit overrides none of the subsequent instructions in response to the conditional execution status updated by the sequencer.

27. (New) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion for reading in a computational instruction;

a decoding portion for decoding the computational instruction that has been read in;

an execution portion for executing the computational instruction in accordance with a decoding of the computational instruction; and

an instruction overriding control circuit for overriding at least one instruction of subsequent instructions that follow the computational instruction in response to a conditional

execution status updated by a sequencer in accordance with the decoding of the computational instruction.

28. (New) The data processing device according to claim 27, wherein the instruction overriding control circuit overrides the at least one instruction by overriding an execution of the at least one instruction in the execution portion.

29. (New) The data processing device according to claim 27, wherein the instruction overriding control circuit overrides the at least one instruction in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.

30. (New) The data processing device according to claim 27, wherein the computational instruction and a first instruction and a second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides either the first instruction or the second instruction in response to the conditional execution status updated by the sequencer.

31. (New) The data processing device according to claim 30, wherein the instruction overriding control circuit overrides either the first instruction or the second instruction in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.

32. (New) The data processing device according to claim 30, wherein neither the first instruction nor the second instruction includes any condition to be overridden.

33. (New) The data processing device according to claim 30, wherein the computational instruction and a first instruction group including a plurality of instruction strings and a second instructional group including a plurality of instructional strings are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides either the first instruction group or the second instruction group in response to the conditional execution status updated by the sequencer.

34. (New) The data processing device according to claim 33, wherein the instruction overriding control circuit overrides either the first instruction group or the second instruction group in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.

35. (New) The data processing device according to claim 33, wherein no instructions included in both the first instruction group and the second instruction group include any conditions to be overridden.

36. (New) The data processing device according to claim 27, wherein the computational instruction and a first instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides the first instruction in response to the conditional execution status updated by the sequencer.

37. (New) The data processing device according to claim 36, wherein the instruction overriding control circuit overrides the first instruction in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.

38. (New) The data processing device according to claim 36, wherein the first instruction does not include any condition to be overridden.

39. (New) The data processing device according to claim 27, wherein the computational instruction and a first instruction group including a plurality of instruction strings are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides the first instruction group in response to the conditional execution status updated by the sequencer.

40. (New) The data processing device according to claim 39, wherein the instruction overriding control circuit overrides the first instruction group in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.

41. (New) The data processing device according to claim 39, wherein no instructions in the first instruction group include any conditions to be overridden.

42. (New) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion for reading in a computational instruction;

a decoding portion for decoding the computational instruction that has been read in;

an execution portion for executing the computational instruction in accordance with a decoding of the computational instruction; and

an instruction overriding control circuit for overriding at least one instruction of subsequent instructions that follow the computational instruction in response to a conditional execution status updated by a sequencer in accordance with the decoding of the computational instruction,

wherein the instruction overriding control circuit overrides the at least one instruction by allowing the fetch portion to skip reading in the at least one instruction.

43. (New) The data processing device according to claim 42, wherein the fetch portion includes a plurality of buffers to override the at least one instruction.

44. (New) The data processing device according to claim 42, wherein the computational instruction and a first instruction and a second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides either an execution of the first instruction in the execution portion or reading in of the second instruction in the fetch portion in accordance with the conditional execution status and a status flag determined by execution of the computational instruction.